

We Claim:

1. A method for fabricating a semiconductor memory having a trench capacitor and a selection transistor, which comprises the steps of:

providing a substrate having a substrate surface with a trench formed therein, the trench having an upper region;

forming an insulation collar in the upper region on a sidewall of the trench;

depositing a dielectric layer functioning as a capacitor dielectric on the insulation collar;

providing a conductive trench filling in the trench;

sinking the conductive trench filling into the trench to a first sinking depth;

removing the dielectric layer from the insulation collar in a region above the first sinking depth;

sinking the conductive trench filling into the trench to a second sinking depth;

uncovering the substrate at the sidewall of the trench above the conductive trench filling resulting in an uncovered sidewall;

growing an epitaxial layer on the uncovered sidewall of the trench;

forming an intermediate layer on the epitaxial layer;

introducing a dopant into the epitaxial layer; and

completing the trench capacitor and the selection transistor.

2. The method according to claim 1, which further comprises removing an upper part of the insulation collar for uncovering the substrate at the sidewall of the trench.

3. The method according to claim 1, which further comprises forming a trench insulation in the substrate and in the trench.

4. The method according to claim 1, which further comprises growing the epitaxial layer such that a facet is formed with an angle of approximately 45 degrees relative to the substrate surface.

5. The method according to claim 4, which further comprises introducing a barrier layer into an annular gap formed by the facet and an upper edge of the insulation collar, the barrier layer preventing dopant diffusions into the sidewall of the trench, the barrier layer being formed by depositing isotropocally a material, impervious to the dopant, at an edge of a trench opening, into the trench and then being etched back anisotropically in a direction perpendicular to the substrate surface.

6. The method according to claim 1, which further comprises removing the insulation collar above a third sinking depth.

7. The method according to claim 6, which further comprises setting the third sinking depth to be greater than the first sinking depth and less than the second sinking depth.

8. A method for fabricating a semiconductor memory having a trench capacitor and a selection transistor, which comprises the steps of:

providing a substrate having a substrate surface with a trench formed therein, the trench having an upper region and a lower region;

providing a first dielectric layer in the lower region of the trench;

forming an insulation collar in the upper region on a sidewall of the trench;

depositing a second dielectric layer on the insulation collar;

providing a conductive trench filling in the trench;

sinking the conductive trench filling into the trench to a first sinking depth;

removing the second dielectric layer from the insulation collar in a region above the first sinking depth;

sinking the conductive trench filling into the trench to a second sinking depth;

uncovering the substrate at the sidewall of the trench above the conductive trench filling resulting in an uncovered sidewall;

growing an epitaxial layer on the uncovered sidewall of the trench;

forming an intermediate layer on the epitaxial layer;

introducing a dopant into the epitaxial layer; and

completing the trench capacitor and the selection transistor.

9. The method according to claim 8, which further comprises removing an upper part of the insulation collar for uncovering the substrate at the sidewall of the trench.

10. The method according to claim 8, which further comprises forming a trench insulation in the substrate and in the trench.

11. The method according to claim 8, which further comprises growing the epitaxial layer such that a facet is formed with an angle of approximately 45 degrees relative to the substrate surface.

12. The method according to claim 11, which further comprises introducing a barrier layer into an annular gap formed by the facet and an upper edge of the insulation collar, the barrier layer preventing dopant diffusions into the sidewall of the trench, the barrier layer being formed by depositing isotropocally a material, impervious to the dopant, at an edge of a trench opening, into the trench and then being etched

back anisotropically in a direction perpendicular to the substrate surface.

13. The method according to claim 8, which further comprises removing the insulation collar above a third sinking depth.

14. The method according to claim 13, which further comprises setting the third sinking depth to be greater than the first sinking depth and less than the second sinking depth.

15. A method for fabricating a semiconductor memory having a trench capacitor and a selection transistor, which comprises the steps of:

providing a substrate having a substrate surface with a trench formed therein, the trench having an upper region;

forming an insulation collar in the upper region on a sidewall of the trench;

providing a conductive trench filling in the trench;

sinking the conductive trench filling into the trench to a first sinking depth;

uncovering the substrate at the sidewall of the trench above the conductive trench filling resulting in an uncovered sidewall;

depositing a dielectric layer directly onto the uncovered sidewall of the trench;

sinking the conductive trench filling into the trench to a second sinking depth;

removing the dielectric layer from the sidewall of the trench;

growing an epitaxial layer on the uncovered sidewall of the trench;

forming an intermediate layer on the epitaxial layer;

introducing a dopant into the epitaxial layer; and

completing the trench capacitor and the selection transistor.

16. The method according to claim 15, which further comprises removing an upper part of the insulation collar for uncovering the substrate at the sidewall of the trench.

17. The method according to claim 15, which further comprises forming a trench insulation in the substrate and in the trench.

18. The method according to claim 15, which further comprises growing the epitaxial layer such that a facet is formed with an angle of approximately 45 degrees relative to the substrate surface.

19. The method according to claim 18, which further comprises introducing a barrier layer into an annular gap formed by the facet and an upper edge of the insulation collar, the barrier layer preventing dopant diffusions into the sidewall of the trench, the barrier layer being formed by depositing isotropically a material, impervious to the dopant, at an edge of a trench opening, into the trench and then being etched back anisotropically in a direction perpendicular to the substrate surface.

20. The method according to claim 15, which further comprises removing the insulation collar above a third sinking depth.

21. The method according to claim 20, which further comprises setting the third sinking depth to be greater than the first sinking depth and less than the second sinking depth.